# Verification of a low Components Nine-Level Cascaded-Transformer Multilevel Inverter in Grid- 

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#### Abstract

The main problem related to cascaded H -bridge cells multilevel inverters (CHBs) is their using of a large number of components, such as switches and DC-sources. Therefore, minimization of components in these kinds of devices is of great importance. Cascaded transformers multilevel inverters (CTMIs) have completely eliminated the need for several DC-sources in CHBs. Thus, minimization of the other components in CTMIs can lead to obtain an optimized structure for multilevel inverters. The present paper introduces a simple and compact structure for transformer based multilevel inverters. Since the number of utilized components in the proposed structure is remarkably reduced, the cost, volume and complexity are minimized. The performance of the suggested inverter has been scrutinized through two different strategies. Firstly, it is tested under condition of supplying a local load, and secondly, employing sample based current control strategy, its performance is inspected when being connected to the grid. In the latter test the leakage inductances of the transformers are utilized to execute the sample based current control strategy, thus, the need for extra filter is eradicated. The feasibility of the suggested topology has been validated by using laboratory-built prototype along with a computeraid simulated model.


Index Terms-multilevel inverter, component reduction, grid-connected converter, sample based current control. Nomenclature

| $v_{s d}$ | Dropped voltage over semiconductor switch and anti-parallel diode |
| :--- | :--- |
| $v_{o s}, v_{d}$ | On-state reverse voltage of an anti-parallel diode and semiconductor switch, respectively. |
| $\Delta v$ | Total dropped voltage of the inverter |
| $V_{m}^{\text {grid }}$ | Peak value of grid voltage |
| $V_{o u t}(n)$ | Voltage value of the $\mathrm{n}^{\text {th }}$ harmonic |
| $r_{s w}, r_{d}$ | Resistance of switch and anti-parallel diode, respectively. |
| $r_{t 1 j}, r_{t 2 j}$ | Primary and secondary winding resistances of the $\mathrm{j}^{\text {th }}$ transformer, respectively. |
| $z_{t 1 j}, z_{t 2 j}$ | Primary and secondary winding impedances of the $\mathrm{j}^{\text {th }}$ transformer, respectively. |
| $i_{l o a d}$ | Load current |
| $i(t)$ | Instantaneous current flowing through a switch or a diode. |
| $i_{d c}$ | current of the DC-source |
| $I_{s j}$ | current of the j th switch |
| $i^{r e f}$ | Reference current |
| $f_{s w}$ | Switching frequency |
| $f$ | Fundamental frequency of the output voltage |
| $\omega$ | $2 \pi f$ |


| $\varphi$ | Phase angle between the output voltage and the load current |
| :--- | :--- |
| $t_{o n}, t_{o f f}$ | Turn-on, and turn-off times of switches, respectively. |
| $C_{o s s}$ | Output capacitance of a switch |
| $a_{0}$ | Zero coefficient of fourier analysis |
| $a_{n}$ | Even coefficient of fourier analysis |
| $k_{j}$ | Transformer ratio of the j th transformer |
| $\Delta P_{s}$ | Power loss of a semiconductor switch with an anti-parallel diode |
| $\Delta P_{c t}$ | Total conductive power loss of semiconductors |
| $\Delta P_{t r}$ | Power losses of the transformers |
| $\Delta P_{f}$ | Switching power loss |
| $\Delta P_{t}$ | Total power loss |
| $P_{r e f}$ | Desired active power (reference active power) |
| $Q_{r e f}$ | Desired reactive power (reference reactive power) |

## 1. Introduction

Multilevel inverters have recently been attracting an increasing amount of attention. The main advantages of these kinds of devises are their ability to convert a higher power and higher quality voltage, minimize dv/dt on switches and load, alleviate electromagnetic interface (LEI), develop lower switching losses and smaller common mode voltage [1-4].

One of the most popular multilevel inverters is cascaded H -bridge cells multilevel inverter (CHB). As it is mentioned in [5], CHB is broadly used in industrial areas such as compressors, synchronous motors, converters and power generation plants.

In spite of the advantages mentioned above, there are some problems related to multilevel inverters. The main problem related to these kinds of devices is an umpteen number of components required to construct them [6-8]. They require several isolated DC sources as well as a large number of switches which seem very difficult to be provided and controlled. Considering the fact that each switch requires a driver circuit and a protection circuit beside it, using a large number of switches in a multilevel structure can make it expensive, bulky, and complicated.

The problem of requiring several DC sources in a multilevel inverter can be addressed by employing transformer based multilevel inverters [9-12]. As shown in Fig.1, these types of multilevel inverters are synthesized with several H-bridge cells. Each cell is connected to the primary winding of a low frequency transformer and the secondary windings of transformers are connected in series. In these types of inverters, which are referred to as Cascaded Transformer Multilevel Inverters (CTMIs), the whole power needed to supply an electrical load is provided by using only one DC unit.

The employed transformers in CTMIs offer some remarkable advantages. For instance, these transformers provide galvanic isolation between load and DC-source, they reduce leakage current in PV application, and by virtue of proper transformer ratio it is possible to convert the voltage from a given level to a desired level. On the contrary, transformers in these inverters cause them to be bulky and expensive. Considering that usually a line transformer is needed in some applications, such as flexible AC transmission systems (FACTS), PV panels, wind turbine, and dynamic voltage restorer (DVR), employing CTMIs in these kinds of applications would be very advantageous. Whereas, the utilized transformers in CTMIs can take responsibilities of the mentioned line transformer. Hence, employing transformers in CTMIs inverter is justifiable when these inverters take role in the mentioned applications

Several topology have been proposed for transformer based multilevel inverters. In [12] a common arm CTMI has been introduced. This topology uses half-bridge cells instead of full-bridge cells, and it includes a common arm that is synthesized with two switches and provides current paths for all the employed transformers. Although this topology brings about significant
components reduction, its main drawback is that the switches placed at the common arm have to suffer a great deal of current. In [13] a symmetric topology of CTMI has been proposed. This topology can approximately halve the number of components required to construct a CTMI. The most unpleasant drawback of the proposed topology in [13] is that the current rating of the switches increases in line with increasing of the output voltage steps. The topology proposed in [14] attempts to reduce the switches count as well. The topology proposed in this reference uses two unidirectional switches and two bidirectional switches in each module. Although respect to [13] the topology suggested in [14] uses higher number of switches, current rating of the utilized switches in this topology is lower than that of the switches in the topology suggested in [13]. The topology suggested in [15], by employing some half-bride cells instead of full-bridge cells, has deservedly reduced the required components counts. Meantime, this topology makes use of a full bridge cell which is connected to the secondary windings of the transformers. Although this cell contributes in increasing the realized voltage levels, it causes the fatal demerit of losing the galvanic isolation feature in this topology. [16] Has proposed using three-phase transformers instated of single-phase transformers in three-phase CTMIs. In this reference the authors have worked out the result that shows employing three-phase transformers instead of singlephase transformers can reduce the size of these kinds of multilevel inverters in three-phase applications. This work is conducted to three-phase applications of the conventional topology, however, the results could be extended to the other topologies as well. CTMI has a considerable ability of facilitating the connection of photovoltaic system to the grid. As an example, [17] Proposes a $\left(2 \times 3^{\mathrm{n}-1}+1\right)$ level CTMI to be used in photovoltaic applications. In the suggested topology in this reference a half bridge cell is added to the conventional topology. The added cell brings about an enhancement in the quality of the developed voltage waveform. Meantime, it reduces two switches. There can be found some other works related to this concept in [18-19].

Motivated by the discussed works above, the present paper introduces a reduced components nine-level single-phase topology for CTMI. Compared to the conventional CTMI, the proposed topology uses a half number of switches to develop a nine-level staircase voltage. Being based on CTMI, it employs only one DC-source and two H-Bridges cells. Thus, we need just eight switches to construct it. In other words, it consists of four switch legs, where each leg consists of two switches, and between the switches in each leg, the primary windings of transformers are connected. Furthermore, we have taken advantage of sample based current control strategy to connect the suggest topology to the grid. To this end, we have used the leakage inductances of the transformers as an interface current filter.

This paper is arranged as follow: in the next section the basic structure of CTMI is presented. In section III, the proposed topology along with its operation principle is illustrated. In section IV the power losses and dropped voltage of the suggested topology are investigated. In section V the proposed topology is compared with the conventional topology and the topologies suggested in [14] and [15]. In order to verify the performance of the suggested topology some computer-aid simulations are performed under Matlab/Simulink environment. The obtained results are shown in section VI. In this section, two scenarios are considered. At the first scenario the inverter shoulders the responsibility of supplying a local load, and in the second scenario, it is responsible to deliver power of a DC unit to an AC grid. In addition, in this section, in two different subsections, both the strategy of sample based current control, which is designed for the proposed topology, and the policy of balancing voltages of the capacitors are illustrated. Additionally, to prove the feasibility of the proposed topology, a laboratory-built prototype has been employed to extract the experimental results. The results of the experimental tests are provided in section VII. Finally, the overall work is concluded in section VIII.

## 2. Conventional cascaded transformers multilevel inverter.

For ease of reference a nine-level topology of the conventional CTMI is shown in Fig. 1. According to this figure, the basic module of CTMI is an H-bridge cell which is connected to a low frequency transformer. The transformer ratio of each cascaded
transformer can be chosen arbitrarily to fulfill a desired voltage magnitude at the output side. There are three main strategies to ascertain the transformer ratio of the transformers. In the first strategy all the utilized transformers have an identical transformer ratio. The topology emerging form this strategy is referred to as symmetric topology. In the second and the third strategies the transformer ratios of the transformers are, respectively, ascertained as binary and ternary. The topologies emerging from the second and the third strategies are both referred to as asymmetric topologies. Comparing these three topologies (symmetric and the two asymmetries), containing an equal number of components, the structure which has transformers with identical transformer ratio would develop a voltage waveform with fewer number of steps. On the contrary, a structure which has transformers with ternary transformer ratio would develop a voltage waveform with higher steps. Although, the quality of the developed voltage can be increased by employing asymmetric strategies, it can deteriorate the other parameters of CTMI. For instance, an asymmetric CTMI would necessitate employing components of higher current rating and switching ability as well as some transformers of different power ratings [18]. Meanwhile, it can increase the power losses of the converter.


Fig. 1. Nine-level configuration of the conventional CTMI.

## 3. Proposed topology

The facility of employing only one DC source, instead of several isolated ones, in cascaded transformers multilevel inverters would help to reach to a simple structure of multilevel inverters. Since, there is no need for the sources to be isolated, they can be connected in series or parallel to form a united source. This is a useful feature because, besides obtaining a simple source arrangement, the inverter would need a simple controlling system.

On the other hand, employing fewer number of switches would help to reach to an optimal structure multilevel inverter. A multilevel inverter with a single DC-source and fewer number of switches and gate drivers requires a simple controlling system with a minimum number of controlling components. Thus, the reduction of components in these types of converters would help to construct a well set and high reliable device with optimized size and cost.

The suggested topology can halve the number of switches and gate drivers which are required to construct a nine-level cascaded transformers multilevel inverter. Having been based on cascaded transformers multilevel inverter, the proposed topology uses only one DC-source to convert the whole power required to supply a local load or grid. The DC-source can be a set of series or parallel connected batteries, PV panels, fuel cells and etc. The suggested topology has been shown in Fig. 2 and the associated switching pattern is tabulated in table 1. According to Fig. 2, the suggested topology consists of four legs and each leg contains two unidirectional switches. Two arms of each transformer are connected to two different legs which are adjacent to each other. It is worth mentioning that two adjacent transformers must have athwart winding on the secondary side (Note the positions of the dots on the transformers' windings in Fig. 2).

The current ratings of the switches are stated in equation (1). According to this equation, the switches in the middle legs provide a current path for two transformers. Thus, each switch in these legs, has to tolerate three times higher current than those in each cell of the conventional CTMI. However, owing to the fact that the switches in the outer legs are connected to only one transformer theses switches do not need to be of high current rating. The Peak Invers Voltage value (PIV) of anti-parallel diodes and Forward Blocking Voltage (FBV) of switches in a multilevel inverter are of great importance, which are necessary to be assessed. PIV and FBV of switches in both, the proposed and the conventional topologies, are the same. As asserted in (2) PIV and FBV of the employed switches in the proposed topology are equal to the input DC voltage value.

Table 1 switching strategy of suggested topology

| levels | Switches status |  |  |  | $V_{\text {out }}=\sum_{i=1}^{4} v_{i}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $S_{1}$ | $s_{2}$ | $S_{3}$ | $S_{4}$ |  |
| 4 | 0 | 1 | 0 | 1 | $\left(\frac{n_{21}}{n_{11}}+\frac{n_{24}}{n_{14}}\right) V_{d c}+\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}$ |
| 3 | 1 | 1 | 0 | 1 | $\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}+\frac{n_{24}}{n_{14}} V_{d c}$ |
|  | 0 | 1 | 0 | 0 | $\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}+\frac{n_{21}}{n_{11}} V_{d c}$ |
| 2 | 1 | 1 | 0 | 0 | $\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}$ |
| 1 | 0 | 0 | 0 | 1 | $\left(-\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}+\frac{n_{21}}{n_{11}} V_{d c}$ |
|  | 0 | 1 | 1 | 1 | $\left(\frac{n_{22}}{n_{12}}-\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}+\frac{n_{21}}{n_{11}} V_{d c}$ |
| 0 | 1 | 0 | 0 | 1 | 0 |
|  | 1 | 1 | 1 | 1 | 0 |
|  | 0 | 0 | 0 | 0 | 0 |
|  | 0 | 1 | 1 | 0 | 0 |
| -1 | 1 | 0 | 0 | 0 | $\left(-\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}-\frac{n_{21}}{n_{11}} V_{d c}$ |
|  | 1 | 1 | 1 | 0 | $\left(\frac{n_{22}}{n_{12}}-\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}-\frac{n_{24}}{n_{14}} V_{d c}$ |
| -2 | 0 | 0 | 1 | 1 | $-\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}$ |
| -3 | 1 | 0 | 1 | 1 | $-\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}-\frac{n_{21}}{n_{11}} V_{d c}$ |
|  | 0 | 0 | 1 | 0 | $-\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}-\frac{n_{24}}{n_{14}} V_{d c}$ |
| -4 | 1 | 0 | 1 | 0 | $-\left(\frac{n_{21}}{n_{11}}+\frac{n_{24}}{n_{14}}\right) V_{d c}-\left(\frac{n_{22}}{n_{12}}+\frac{n_{23}}{n_{13}}\right) \frac{V_{d c}}{2}$ |

$$
\left.\begin{array}{l}
I_{S 1}=\left(\frac{n_{21}}{n_{11}}\right) S_{1} \cdot I_{\text {Load }}  \tag{1}\\
I_{S 2}=\left(\frac{n_{21}}{n_{11}}+\frac{n_{22}}{n 12}\right) S_{2} \cdot I_{\text {Load }} \\
I_{S 3}=\left(\frac{n_{23}}{n_{13}}+\frac{n_{24}}{n 14}\right) S_{3} \cdot I_{\text {Load }} \\
I_{S 4}=\left(\frac{n_{24}}{n_{14}}\right) S_{4} \cdot I_{\text {Load }} \\
S 1, S 2, S 3, S 4 \in\{0,1\}
\end{array}\right\}\left\{\begin{array}{l}
F B V=V_{d c} \\
P I V=V_{d c}
\end{array}\right.
$$



Fig. 2. Proposed topology

## 4. Investigation of power losses and dropped voltage

In this section, the power losses and the dropped voltage of the proposed topology are investigated. The voltage drop in an inverter can appear a consequence of two main issues. The first issue is the existing of some impedances that appear along the current path, and the second issue is the existing of an on-state reverse voltage that appears when a semiconductor switch or diode is in the on state. The general equation of dropped voltage over a semiconductor switch and that of the dropped voltage of the suggested topology are shown in (3) and (4) respectively [20]:

$$
\begin{align*}
& \left\{\begin{array}{l}
v_{d}+r_{d} i(t) 0<\omega t<\varphi \\
v_{o s}+r_{t} i(t) \varphi<\omega t<\pi
\end{array}\right.  \tag{3}\\
& \Delta v=\sum_{j=1}^{4}\left(k_{j}^{-2} z_{t 1_{j}}+z_{t 2_{j}}\right) i_{l o a d}+\sum_{j=1}^{4} v_{s d_{j}} k_{j}^{-1}
\end{align*}
$$

The power losses related to semiconductor switches can be divided into two categories. The first is the power loss which is an outgrowth of the resistive impedance and an on-state voltage which appears along the path of the current. This power loss is referred to as conductive power loss. Equation (5) describes conductive power loss in general, and equation (6) presents conductive power loss of the proposed topology. The second is the power loss that stems from the switching action of switches in a power electronic based device. This power loss is known as switching power loss [21]. Equation (7) suggests the switching power loss of the proposed topology.

It is universally acknowledged that all the components in a power electronic based device can bring about a power loss. According to this reality, the other components of the suggested topology such as non-ideal transformers can also cause some power losses. The power losses which apear due to the presence of the transformers are demonstrated in (8). The total power loss is calculated by (9).

$$
\begin{align*}
& \Delta P_{s}=\frac{1}{\pi}\left(\int_{0}^{\varphi}\left(v_{s d}(t) i(t)+r_{d} i(t)^{2}\right) d t+\int_{\varphi}^{\pi}\left(v_{o s}(t) i(t)+r_{s w} i(t)^{2}\right) d t\right)  \tag{5}\\
& \Delta P_{c t}=\sum_{j=1}^{8} \Delta P_{s_{j}} \tag{6}
\end{align*}
$$

$$
\begin{align*}
& \Delta P_{f}=v_{d c} f_{s w} \sum_{j=1}^{8}\left(\left(t_{o f f}+t_{o n}\right) I_{s_{j}}+C_{\text {oss }}\right)  \tag{7}\\
& \Delta P_{t r}=i_{\text {Load }}^{2} \sum_{j=1}^{4}\left(k_{j}^{-2} r_{t 1_{j}}+r_{t 2_{j}}\right)  \tag{8}\\
& \Delta P_{t}=\Delta P_{c t}+\Delta P_{f}+\Delta P_{t r} \tag{9}
\end{align*}
$$

## 5. Comparison

Two new topologies in term of CTMI have been proposed in [14], and [15]. For ease of reference two symmetric nine-level configurations for these two topologies are shown in Fig. 3 (a) and (b). The topology in [14], by virtue of two capacitors, divides the voltage of the DC-source by half. Through this manner it provides a square AC voltage to be used as the input voltage of the transformers. According to Fig. 3 (a) the topology suggested in [14] reduces the components count respect to the conventional topology. Although the topology suggested in [15] has deservedly reduced the number of switches, it has lost the most important feature of providing galvanic isolation. Table 2 tabulates the required components to synthesize a nine-level configuration of the proposed topology, the conventional topology, and the topologies suggested in [14] and [15].

In order to compare the electrical features of these four topologies, three main electrical characteristics of them have been appraised. To this end, firstly, the overall dropped voltage over the semiconductors is appraised. Secondly, the conductive power losses of the utilized semiconductors are assessed. For the sake of brevity, since all the aforementioned topologies include the same identical transformers, assessing the power losses and the dropped voltage arisen from them are avoided. Thirdly, the switching power losses are considered.

The equations of the dropped voltage and the power loss related to the proposed topology are, respectively, cited in equations (4) and (9). These equations for the conventional topology and the topologies of [14] and [15] can be obtained by tracing the current paths in these topologies. Table 3 lists the switches characteristics that are considered to extract comparison results. All the switches employed, are considered to be commercially available and all the data listed, are extracted from their datasheets. Since switches located at the two middle legs of the proposed topology have to tolerate three times higher current than those located at the two outer legs, two different types of switches considered for the proposed topology. These two types differ in current ratings. This also is the case for switches utilized in topologies of [14] and [15].

In order to precisely do the comparison, five current values of $2(A), 4(A), 6(A), 8(A)$, and $10(A)$ are assumed to be provided by the considered topologies. Fig. 4 (a) shows the overall dropped voltage over the semiconductors of the four compared topologies. According to these figures the proposed topology offers the lowest dropped voltage. Since in the topology of [14] the current passes through some series connected switches, this topology has the highest voltage drop among the compared topologies. This is also the case when comparing the conductive power losses of these four topologies as shown in Fig. 4 (b). As to switching power loss, since the four unidirectional switches in [14] operate at the frequency of the output voltage (50Hz), this topology has the lowest switching power loss among the topologies under comparison as exhibited in Fig 4. (c). on the contrary, whereas all the switches in the conventional topologies operated at the ascertained switching frequency this topology has the highest switching power loss. In this term the proposed topology comes seconds and the topology in [15] comes third. It is to be mentioned that the input DC voltage is assumed to be 200 v and the switching frequency is considered to be 5 KHz .

Table 2. comparison

| topologies | Numbers <br> of switches | Numbers of <br> switch drivers | Numbers Transformers <br> of equal power rating | FBV \& PIV <br> of switches |
| :---: | :---: | :---: | :---: | :---: |
| conventional | 16 | 16 | 4 | Vdc |
| $[14]$ | 12 | 8 | 4 | Vdc |
| $[15]$ | 10 | 10 | 3 | Vdc |
| The proposed | 8 | 8 | 4 | Vdc |

Table 3. characteristics of the considered switches

| Switch type | $\mathrm{R}_{\mathrm{DS}}$ | $\mathrm{V}_{\mathrm{os}}$ | Drain-source voltage | Current rating |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $(\Omega)$ | $(\mathrm{v})$ | $(\mathrm{V})$ | Turn-on time <br> $(\mathrm{A})$ | Turn-off time <br> $(\mathrm{ns})$ | $\mathrm{C}_{\mathrm{oss}}$ |
|  | $(\mathrm{nF})$ |  |  |  |  |



Fig. 3. (a) Proposed topology in [14]. (b) Proposed topology in [15]


Fig 4. (a) Total dropped voltage over the semiconductors. (b). Total conductive power loss of the semiconductors. (c) Total switching power losses of the semiconductors.

## 6. Simulation results

In this section the performance of the proposed topology has been investigated through a model simulated under mathlab/Simulink environment. The specifications of the simulated model are shown in table 4. The simulated nine-level multilevel inverter model is considered to supply an RL load of 0.9 power factor $(50 \Omega+75 \mathrm{mh})$ with nominal voltage and frequency of 220 v and 50 Hz , respectively. Fig 5 (a) shows the output voltage of the suggested topology in no load condition. Fig 5 (b) shows the output voltage and load current when it supplies the mentioned RL load. Furthermore the performance of the suggested topology in the presence of a pure resistive load of $50 \Omega$ is shown in Fig. 5 (c). Scrutinizing these three figures it is seen that the high-frequency harmonics vanish as the power factor of the load increases, this phenomena is illustrated by referring to Fig. 6. As shown in this figure, each transformer contains two leakage inductances in its primary and secondary sides. The primary inductance can be transferred to the secondary side, so that, the two inductances can be modeled as an overall leakage inductance at the secondary side. Since the secondary sides of the transformers are connected in series, their leakage inductances can be modeled as a united inductance which is connected to the load in series. As shown in Fig. 6 (c) and according to (10) the high-frequency components of the input voltage cause the leakage impedance to be drastically high ( $\left.2 \pi n f L_{s_{t}} \gg R_{\text {load }}\right)$. Hence, as the load power factor increases the high-frequency components of voltage disappear at the output. On the contrary, as the inductive characteristic of the load increases (power factor decreases), for the high-frequency components the inductive characteristic dominates the resistive characteristic of the load, so that, the high-frequency components will appear at the output voltage.

FFT analysis of the output voltage under the three mentioned loading conditions are depicted in Fig. 5 (d), (e), and (f). According to these FFT analyses and equation (10), since under pure resistive loading condition the higher-frequency harmonics are mitigated, the inverter offers an output voltage of higher quality in this condition. What is more, according to these figures the dominant harmonics appear around switching frequency (the switching frequency is considered to be 5 KHz )

Additionally, in order to assume a loading condition under which the proposed inverter provides both active and reactive powers, the loading condition of the aforementioned resistive-inductive loads are taken into consideration. The currents of the switches in the two outer legs and those of the switches in the two middle legs are, respectively, shown in Fig. 5 (g) and (h). Mealtimes, these figures exhibit the FBV values of the switches and PIV values of the anti-parallel diodes. As stated earlier and illustrated by (1) the switches in the middle legs tolerate three times higher current respect to those in the outer legs. However, as indicted in (2), in the case of FBV and PIV, all the switches and anti-parallel diodes withstand the same voltage which is equal the input DC-voltage value.

In order to deal with reactive power and to provide path for the reverse current a capacitor is connected in parallel to the DCsource in the conventional CTMI as shown in Fig. 1. The two capacitors in the proposed topology ( C 1 and $\mathrm{C} 2 \mathrm{in} \mathrm{Fig}. \mathrm{2)} \mathrm{can}$ shoulder the same task. The load current along with the capacitor current, under the mentioned resistive-inductive loading condition (supplying active and reactive power), are shown in Fig. 5 (j)

Table 4. Specifications of the simulated model

| Transformers | Winding 1 parameters |  |  | Winding 2 parameters |  |  | Magnetization resistance and inductance |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{V} 1(\mathrm{rms})$ | $\mathrm{R} 1(\mathrm{~m} \Omega)$ | $\mathrm{L} 1(\mathrm{mH})$ | $\mathrm{V} 2(\mathrm{rms})$ | $\mathrm{R} 2(\mathrm{~m} \Omega)$ | $\mathrm{L} 2(\mathrm{mH})$ | $\mathrm{Rm}(\Omega)$ | $\mathrm{Lm}(\mathrm{H})$ |  |  |
| $\mathrm{T} 1, \mathrm{~T} 4$ | 24 | 2.304 | 0.293 | 78 | 24.336 | 3.1 | 576 | 1.8335 |  |  |
| $\mathrm{~T} 2, \mathrm{T3}$ | 12 | 0.576 | 0.073 | 78 | 24.336 | 3.1 | 144 | 0.45837 |  |  |
| $\mathrm{C} 1, \mathrm{C} 2=2200 \mu \mathrm{~F}$ |  |  |  |  |  |  |  | $\mathrm{Vdc}=24 \mathrm{~V}$ |  |  |



Fig. 5. Simulation results of the output voltage, load current, FFT analyses, and switches voltages \& currents. (a) Output voltage in no load condition, (b) output voltage and load current when supplying the RL load (c) output voltage and load current when supplying the pure resistive load. (d) FFT analysis of the output voltage in no load condition. (e) FFT analysis of the output voltage when supplying the RL load. (f) FFT analysis of the output voltage when supplying the pure resistive load. (g) Voltages and currents of the switches of the two outer legs. (h) Voltages and currents of the switches of the two middle legs. (j) Load and capacitor currents when providing active and reactive power (resistive-inductive loading condition).


$$
V_{i n_{j}}=\sum_{n=1}^{m} a_{n_{j}} \sin (n \omega t)
$$

(a)

(c)
(b) $V_{t_{j}}=k_{j} V_{i n_{j}}$

$$
L_{s_{j}}=L_{s_{2 j}}+k_{j}^{2} L_{S_{1} j}
$$

$$
V_{t_{t}}=\sum_{j=1}^{4} \sum_{n=1}^{m} k_{j} a_{n_{j}} \sin (n \omega t)
$$

$$
L_{S_{t}}=\sum_{j=1}^{4} L_{S_{j}} \quad V_{\text {out }}=\sum_{j=1}^{4} V_{\text {out }_{j}}
$$

. (c) Simplified model of the transformers in the proposed topology.

$$
\begin{equation*}
V_{\text {out }}(n)=\frac{\sqrt{R_{\text {load }}^{2}+\left(2 \pi n f L_{\text {load }}\right)^{2}}}{\sqrt{R_{\text {load }}^{2}+\left(\left(L_{\text {load }}+L_{s_{t}}\right)(2 \pi n f)\right)^{2}}}\left(\sum_{j=1}^{4} k_{j} a_{n_{j}} \sin (n \omega t)\right) \tag{10}
\end{equation*}
$$

## A. Sample based current control strategy

As we know, multilevel inverters are playing a significant role in renewable energy resources systems and micro-grid applications. Where, they deliver the power generated by renewable resources to the grid [22-24]. Since, transformers are predominately used to connect multilevel inverters to the grid, a transformer based inverter can be a suitable alternative in these kinds of applications. Furthermore, the leakage inductances of the transformers can be used as a current filter [25]. Thus, the need for an extra filter can be eradicated. Another benefit of using transformers is that they can provide a galvanic isolation [2627]. The present section scrutinizes the performance of grid-tied model of the suggested topology. The Specifications of the model and grid are shown in table 5 and the scheme of such a system is depicted in Fig. 7 (a). The strategy of sample based current control has been adopted to deliver a given amount of active power to the grid through the proposed multilevel inverter. The active power is assumed to be a varying power from 15 kw to 25 kw . Meanwhile, the leakage inductance of the transformers have been used as a current filter.

The position of grid voltage respect to the levels is depicted in Fig. 7 (b). According to this figure at each instance of the time the gird voltage is surrounded by two possible levels of the inverter output voltage. One of the surrounding level is in the upper position (upper level), and the other one is in the lower position (lower level). These two levels are used to get the injected current follow the reference current. To this end, at the end of each switching period, the injected current is compared with the reference current. On condition that the injected current value is higher than that of the reference current the switching pattern of the lower level will be executed at the next switching period, or else, the switching pattern of the upper level should be executed. For instance, as shown in Fig. 7 (b), during time interval from 0.007 to 0.008 second the grid voltage is surrounded by two levels (level 3 and level 2), where, level 3 is the upper level and level 2 is the lower level. So, during the mentioned time interval, if in a certain switching period the measured current exceeds the reference current, the switching pattern related to level 2 (lower level) will be executed at the next switching period. This will pull down the injected current to keep it somewhere near to the reference current. On the contrary, on condition that the measured current is lower than the reference current, the switching pattern related to level 3 (upper level) will be employed at the next switching period. This will rise up the injected current to catch up with the reference current.

Assuming that the power losses are negligible, the reference current can be obtained from (11) [28]. Fig. 7 (a) shows the procedure of obtaining the reference current. As shown, the controlling system needs a PLL to determine the frequency of the grid. K1 and K2, are gains that are used to scale down the grid and DC voltages in order to make them compatible with the signal processing unit. The reference active power ( $P_{r e f}$ ) and the reference reactive power ( $Q_{r e f}$ ) can be ascertained by adopting droop-control approaches in micro grid applications [23-31] or various methods of maximum power point tracking (MPPT) in PV or wind turbine applications etc. [32-35]. Fig. 8 (a) shows both the reference current and the injected current to the grid which is a simulation result of the simulated model. In order to have unity power factor, in the case of angle the injected current should vary in line with the grid voltage. This issue is depicted in Fig. 8(b). Finally the FFT analysis of the injected current is shown in Fig. 8 (c).

$$
\begin{equation*}
i^{r e f}(t)=I_{m}^{r e f} \sin (\omega t+\alpha)=\frac{2 P_{r e f}}{V_{m}^{\text {grid }}} \sin (\omega t)-\frac{2 Q_{\text {ref }}}{V_{m}^{\text {grid }}} \cos (\omega t) \tag{11}
\end{equation*}
$$



Fig. 7. (a) Grid tied model. (b) grid voltage and surrounding levels


Fig.8. Simulation results of grid-tied model. (a) Reference current and injected current. (b) Injected current and grid voltage. (c) FFT analysis of the injected current

Table 5. specifications of grid-tied model

| transformers | Winding 1 parameters |  |  | Winding 2 parameters |  |  | Magnetization resistance and inductance |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | V1(rms) | R1( $\Omega$ ) | L1(mH) | V2(rms) | R2(m) | L2(mH) | $\mathrm{Rm}(\Omega)$ | Lm(H) |
| T1,T4 | 750 | 0.1125 | 2.69 | 83 | 1.38 | 0.0329 | 28125 | 89.525 |
| T2,T3 | 375 | 0.028 | 0.67 | 83 | 1.38 | 0.0329 | 7031.3 | 22.381 |
| $\mathrm{L}_{\mathrm{f}}(\mathrm{H})$ | $2 *\left(0.00269 * 9^{-2}+3.289 * 10^{-5}\right)+2\left(0.028 *(4.5)^{-2}+3.289 * 10^{-5}\right)=0.003$ |  |  |  |  |  |  |  |
| $\mathrm{C}_{1}=\mathrm{C}_{2}=4700 \mu \mathrm{~F}$ |  | $\mathrm{V}_{\mathrm{dc}}=750 \mathrm{~V}$ | $\mathrm{C}_{\mathrm{f}}(\mathrm{F})=460 \mu \mathrm{~F}$ |  | $\mathrm{P}_{\text {ref }}=25 \mathrm{kw}$ |  | Vt [Grid] $=220 \sqrt{2} \sin (314 \mathrm{t})$ |  |

## B. Capacitors voltage balancing strategy

To realize a staircase voltage of symmetric levels postulates having a balanced voltage over the two capacitors. To this regard it is necessary to control the mid-point voltage of the two capacitors. Referring to table 1 we realize that only the switching patterns related to the switches $S_{2}, S_{2}^{\prime}, S_{3}$, and $S_{3}^{\prime}$ affect the mid-point voltage, whereas they provide current paths which go through the capacitors, while switches $\mathrm{S}_{1}, \mathrm{~S}^{\prime}, \mathrm{S}_{4}$, and $\mathrm{S}^{\prime}{ }_{4}$ provide current paths which go, directly, through the DC-source. Also going through this table we discern that the switching patterns related to the levels of $2,-2,3,-3,4$, and -4 cause an equal current to be flow through the capacitors. Therefore they have no effect on the appeared imbalance voltage in the mid-point. On the contrary, in the switching patterns related to levels 0,1 , and -1 at each instance of the switching period only one of the two capacitors is responsible to provide the current paths. This leads to an inequality of voltage over the capacitors. As shown in table 1 there are two possible switching patterns for each levels of 1 and -1 , also four possible patterns for level zero. The mentioned approaches are depicted in Fig. 9 with meticulous details. In order to, briefly, show the current paths which affect voltage balance of the two capacitors, only the two proper patterns for level zero and level 1 together with switching patterns of levels 2 and 3 are depicted in these figures. The switching patterns of the other levels and related current paths could be projected by referring to table 1.

According to Fig. 9, in the four shown patterns for levels zero and 1 only one of the two capacitors shoulders the responsibility of providing current paths which go through switches $S 2, S 3$ or $S^{\prime} 2$ and $S^{\prime} 3$. This would lead to an inequality of voltage over the capacitors. Also according to this figure in levels 2 and 3 the two capacitors equally provide current paths. So it makes sense that the voltages of the capacitors remain equal in these levels. This is, also, the case in levels $-2,-3,-4$, and 4 (not shown). In order to have the two capacitors get an equal voltage, the two possible switching patterns should be executed in a successive switching period when realizing levels 1 and -1 . Also two switching patterns out of the four possible patterns can be adopted to realize zero level and equal voltages over the capacitors. It is to be mentioned that the two selected patterns for zero level must differ in the states of switches $\mathrm{S} 2, \mathrm{~S}^{\prime} 2, \mathrm{~S} 3$, and $\mathrm{S}^{\prime} 3$. On the contrary, the states of switches $\mathrm{S} 1, \mathrm{~S}^{\prime} 1, \mathrm{~S} 4$, and $\mathrm{S}^{\prime} 4$ are immaterial in the selected patterns. However in order to have a lower switching frequency it is desirable to have constant states for these switches.


Fig. 9.switching patterns and current paths. (a) and (b) the two proper patterns and current paths to realize level zero. (c) and (d) the two patterns to realize level one. (e) and (f) switching patterns of level two and level three.

## 7. Experimental result

In order to prove the feasibility of the suggested topology, a laboratory-built model has been employed. Fig. 10 shows a photo of the employed prototype and table 6 lists the specifications of the model in different modes. DSP-IDC28335Kv2 has been adopted to compute the signals of the switches gates drivers and two series connected batteries of 12 v and 60 Ah are employed as the DC-voltage supplying unit.

The prototype has gone under different tests. Firstly, its output voltage has been obtained under no load condition. Fig. 11(a) shows the nine-level staircase output voltage resulted from this test. It is to be noted that, a sinusoidal voltage with peak value of $220 \sqrt{2} \mathrm{~V}$ and frequency of 50 Hz has been assumed as the desired output voltage. As shown, there is about 10 v dropped voltage in no load condition that arises from the existence of the on-state reverse voltages of the switches. Secondly, the prototype has been examined when it supplies a pure resistive load of 400 w, the result is shown in Fig. 11 (b). As depicted in the simulation section and illustrated by (10), when supplying a pure resistive load the suggested inverter offers a more sinusoidal output voltage. Additionally, the prototype performance has been scrutinized when it is loaded by a resistive-inductive load of 250 w with lag power factor of 0.8 . The result has been shown in Fig. 11 (c). Furthermore in order to investigate the effect of the load current on the switches the current of the four lower switches under the mentioned loading condition are shown in Fig. 11 (d) and (e). The input current for this load is also shown in Fig. 11 (f). As mentioned in the simulation part, according to Fig. 11 (d) and (e) the switches located in the two inner legs tolerate three times higher current than those in the outer legs. In order to provide more clarity, dynamic behavior of the suggested topology is also tested. Fig. 11 (g) shows behavior of the prototype inverter when it responses to a load change from no load to a pure resistive load of 400 w . Meanwhile Fig. 11(h) depicts the response to the condition under which the load changes from 150 w pure resistive load to a resistive-inductive load of 150 w with a lag power factor of 0.9 .

The other important experimental test that the prototype passed successfully, was the test that accomplished under gird tie condition. In this test, by adopting sample based current strategy, the proposed structure shouldered the responsibility of delivering 800 w active power to the grid. The result of this test is demonstrated in Fig. 11 (j). As shown, the voltage of the infinite grid is $220 \sqrt{2} \sin 100 \pi t$. In this test the voltage magnitude of DC-source was adjusted to be 80 v . As shown the injected current, in the case of phase, is in line with the grid voltage. This indicates that the proposed topology has an acceptable performance in this term.

Experimental FFT analysis of the output voltage and load current are, respectively, provided in Fig. 11 (k) and (l). As shown in Fig. 5 (d) and (e) in the simulation part, the low frequency harmonics values of the output voltage are insignificant and the most noticeable harmonics are of higher frequency which emerge around multiple of the switching frequency. Since switching frequency is far from the fundamental frequency these harmonics can easily be eradicated by some small filters. The experimental result depicted in Fig. 11 (k) lends credence to the FFT analysis obtained in the simulation part. Extracting the harmonic values from Fig. 11 (k) THD values of the output voltage is calculated to be $12.9 \%$. As to FFT analysis of the load current, since the leakage inductances of the transformers and the inductive feature of the load act as current filters, the load current has a distortion free sinusoidal waveform. Hence, as shown in Fig. (l), no significant harmonic emerges in the FFT analysis of the load current. Thus THD value of the load current is zero.


Table 6. Specifications of prototype model

| Parameters | supplying local load | Grid-tie mode |
| :--- | :--- | :--- |
| Input voltages of $\mathrm{T}_{1} \& \mathrm{~T}_{4}$ | 24 V | 80 V |
| Input voltages of $\mathrm{T}_{2} \& \mathrm{~T}_{3}$ | 12 V | 40 V |
| Leakage impedance of transformers [R2 L2] | $[1.2 \Omega+0.4 \mathrm{mH}]$ | $[0.36 \Omega+2.8 \mathrm{mH}]$ |
| Magnetization resistance and inductance [Rm Lm] | $[1440 \Omega 4.5 \mathrm{H}]$ | $[1440 \Omega 4.5 \mathrm{H}]$ |
| Transformer ratio of $\mathrm{T}_{1} \& \mathrm{~T}_{4}\left(N_{11} / N_{21} \& N_{14} / N_{24}\right)$ | 0.31 | 1 |
| Transformer ratio of $\mathrm{T}_{2} \& \mathrm{~T}_{3}\left(N_{12} / N_{22} \& N_{13} / N_{23}\right)$ | 0.155 | 0.5 |
| Switching frequency | 5 kHz | 35 kHz |
| $\mathrm{C}_{1} \& \mathrm{C}_{2}$ | $4600 \mu \mathrm{~F}$ | $4600 \mu \mathrm{~F}$ |




Fig 11. Experimental results. (a) output voltage in no load condition. (b) load current and output voltage when supplying the pure resistive load. (c) load current and output voltage when supplying the resistive-inductive load. (d) and (e) switches current. (f) Input current. (g) dynamic response from no load to pure resistive load. (h) dynamic response from pure resistive load to inductive-resistive load. (j) injected current and the grid voltage when inverter injects current to the grid. (k), and (l) FFT analysis of the output voltage and load current respectively.

## 8. Conclusion

This paper put forth a novel nine-level topology for transformer based multilevel inverters. The proposed topology can deservedly reduce switches count of a nine-level single-phase multilevel inverter. To prove the feasibility of the suggested topology, by using a model simulated under Mathlab/Simulink environment and a laboratory-built prototype, it went under two different tests. Firstly, its performance was assessed when supplying a local load. The load was assumed to be either a pure resistive load or a resistive-inductive load. Secondly, employing sample based current control strategy, its performance was inspected under grid-tied condition. By employing a simulated model in the latter test, the proposed topology took the responsibility of delivering an assumed active power of 15 kW , and 25 kW to the grid. In the experimental test the power value injected to the grid was considered to be 800 w . Since the CTMIs mostly use only one DC-source they are a competent candidate in microgrid and PV application. Being based on CTMIs, the proposed topology employs fewer numbers of components and offers the same advantages as the conventional topology does. When adopting the sample based current control strategy in gridtie applications an inductive element is required to be located between the converter and the grid. In this paper the leakage inductances of the transformers were used as the inductive filter. This facilitated executing the sample based current control strategy and consequently the need for an extra filter is eradicated. The other advantage of using transformers was their providing a galvanic isolation. To sum up, the accomplished tests verified the feasibility and viability of the suggested topology.

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